IN THE CLAIMS:

1. Claims 1-15: (Canceled)

16. (Currently amended) A memory device having a core that includes memory cells, the memory device comprising:

a clock receiver circuit to receive an external clock signal;

a delay locked loop circuit coupled to the clock receiver circuit, wherein:

during a first power mode the delay locked loop circuit and the clock receiver circuit are turned on; and

during a second power mode, the delay locked circuit is turned off.

17. (Previously presented) The memory device of claim 16, wherein the second power mode is a power down mode.

18. (Previously presented) The memory device of claim 17, wherein during the second power mode, the clock receiver circuit is turned off.

19. (Currently amended) The memory device of claim 18, further including a first control line, coupled to the clock receiver circuit and the delay locked loop circuit, wherein, during the second power mode, the delay locked loop circuit and the clock receiver circuit are turned off using the first control line.

20. (Currently amended) The memory device of claim 16, wherein during a third power mode, the delay locked loop circuit is in a low power configuration and the clock receiver circuit is turned on.

21. (Previously presented) The memory device of claim 20, wherein the third power mode is a nap mode.

22. (Previously presented) The memory device of claim 20, wherein a resynchronization time of the delay locked loop circuit in the low power configuration is less than a resynchronization time of the delay locked loop circuit in the second power mode.

23. (Previously presented) The memory device of claim 16, wherein the first power mode is a standby power mode.

24. (Previously presented) The memory device of claim 23, further including an input to receive control information that specifies a transition from the standby power mode to an active mode, wherein a sense operation is performed during the active mode, and wherein a row of the memory cells is sensed during the sense operation.

25. (Previously presented) The memory device of claim 24, wherein during the active mode, a clock signal output from the delay locked loop circuit is electrically coupled to sense control logic, and wherein a row command instructs the sense control logic to perform the sense operation.

26. (Previously presented) The memory device of claim 24, further including a receiver circuit to receive data, wherein the receiver circuit is turned on after a delay time in response to receiving a write command, the receiver circuit to receive data to be written to the row of the memory cells.

27. (Previously presented) The memory device of claim 26, further including a write control circuit, coupled to the receiver circuit, wherein a clock signal generated by the delay locked loop circuit is provided to the write control circuit in response to receiving the write command.

28. (Previously presented) The memory device of claim 26, wherein the data to be written to the row of the memory cells is written to a location within the row, wherein the location is specified by a column address.

29. (Previously presented) The memory device of claim 26, further including a register to program the delay time.

30. (Previously presented) The memory device of claim 24, further including a read control circuit, coupled to the core, wherein the read control circuit is turned on in response to receiving a read command that specifies an access of data from the row of the memory cells.

31. (Previously presented) The memory device of claim 30, wherein a clock signal generated by the delay locked loop circuit is provided to the read control circuit in response to receiving the read command.

32. (Withdrawn) A memory device comprising:

a memory core including memory cells;

a clock receiver circuit to receive an external clock signal;

a delay locked loop circuit coupled to the clock receiver circuit, wherein:

during a first power mode the delay locked loop circuit and the clock receiver circuit are turned on; and

during a second power mode, the delay locked loop circuit is turned off;

an input to receive control information that specifies a transition from the first power mode to an active mode, wherein the memory device performs a sense operation on a specified row of memory cells during the active mode;

a receiver circuit to receive data to be written to memory cells sensed during the sense operation, wherein the receiver circuit is turned on after a latency period in response to receiving a write command; and

a register to program the latency period.

33. (Withdrawn) The memory device of claim 32, wherein during the second power mode, the clock receiver circuit is turned off.

34. (Withdrawn) The memory device of claim 32, further including a first control line, coupled to the clock receiver circuit and the delay locked loop circuit, wherein, during the second power mode, the delay locked loop circuit and the clock receiver are turned off using the first control line.

35. (Withdrawn) The memory device of claim 32, wherein during a third power mode, the delay locked loop circuit is in a low power configuration and the clock receiver is turned on.

36. (Withdrawn) The memory device of claim 35, wherein a resynchronization time of the delay locked loop circuit, when in the low power configuration, is less than a resynchronization time of the delay locked loop circuit when in the second power mode.

37. (Previously presented) A method of operation of a memory device having a core of memory cells, the method comprising:

receiving a command that specifies a power down mode;

turning off a delay locked loop circuit in response to the command that specifies the power down mode; and

operating the memory device in a standby power mode, wherein the delay locked loop circuit is turned on in the standby mode.

38. (Previously presented) The method of claim 37, wherein during the power down mode, a clock receiver circuit is turned off.

39. (Previously presented) The method of claim 37, further including operating the memory device in a nap mode, wherein during the nap mode, the delay locked loop circuit is in a low power configuration.

40. (Previously presented) The method of claim 39, wherein a resynchronization time of the delay locked loop circuit in the low power configuration is less than a resynchronization time of the delay locked loop circuit in the power down mode.

41. (Previously presented) The method of claim 37, further including:

transitioning from the standby power mode to an active mode; and

sensing a row of the memory cells during the active mode.

42. (Previously presented) The method of claim 41, further including:

receiving a write command; and

in response to the write command, turning on a receiver circuit to receive data after a period of time transpires, wherein the data is written to the row of memory cells.

43. (Previously presented) The method of claim 42, further including programming the period of time using a register.

44. (Previously presented) The method of claim 41, further including:

receiving a read command; and

in response to the read command, turning on a read pipeline to output data from the memory device.

45. (Withdrawn) A memory device comprising:

a memory core including memory cells;

a delay locked loop circuit wherein:

during a standby power mode, the delay locked loop circuit is turned on; and

during a power down mode, the delay locked loop circuit is turned off;

an input to receive control information that specifies a transition from the first power mode to an active mode, wherein the memory device performs a sense operation on a specified row of the memory cells during the active mode;

a clock receiver circuit, coupled to the delay locked loop circuit, to receive an external clock signal, wherein the clock receiver circuit is turned on during the standby power mode;

a first control line, coupled to the clock receiver circuit and the delay locked loop circuit, wherein, during the power down mode, the delay locked loop and the clock receiver are turned off using the first control line; and

a receiver circuit to receive data, after a latency period transpires, in response to receiving a write command, the data to be written to the row of the memory cells.

46. (Withdrawn) The memory device of claim 45, wherein during a nap power mode, the delay locked loop circuit is in a low power configuration and the clock receiver circuit is turned on.

47. (Withdrawn) The memory device of claim 46, wherein a resynchronization time of the delay locked loop circuit in the low power configuration is less than a resynchronization time of the delay locked loop circuit in the power down mode.

48. (Withdrawn) The memory device of claim 45, further including a register to program the latency period.

49. (Withdrawn) The memory device of claim 45, wherein the receiver circuit is turned on before the data arrives.

50. (Withdrawn) A memory device comprising:

a memory core including memory cells;

a delay locked loop circuit wherein:

during a nap power mode, the delay locked loop is in a low power configuration; and

during a standby power mode, the delay locked loop circuit is turned on;

a clock receiver circuit, coupled to the delay locked loop circuit, to receive an external clock signal, wherein the clock receiver circuit is turned on during both the standby power mode and the nap power mode;

an input to receive control information that specifies a transition from the standby power mode to an active mode, wherein the memory device performs a sense operation on a specified row of the memory cells during the active mode; and

a receiver circuit to receive data, after a latency period transpires, in response to receiving a write command, the data to be written to the row of the memory cells.

51. (Withdrawn) The memory device of claim 50, wherein during a power down mode, the delay locked loop circuit is turned off.

52. (Withdrawn) The memory device of claim 51, wherein a resynchronization time of the delay locked loop circuit when in the nap power configuration is less than a resynchronization time of the locked loop circuit when in the power down mode.

53. (Withdrawn) The memory device of claim 50, wherein the receiver circuit is turned on before the data arrives.

54. (Withdrawn) The memory device of claim 50, further including a register to program the latency period.

55. (Withdrawn) A memory device, comprising:

a clock receiver circuit adapted to receive a clock signal;

a phase compensation circuit coupled to the clock receiver circuit and a control signal line, the phase compensation circuit configurable to transition from a first power mode to a second power mode in response to a control signal received from the control signal line.

56. (Withdrawn) The memory device of claim 55, wherein the phase compensation circuit is a delay locked loop circuit.

57. (Withdrawn) The memory device of claim 55, further comprising:

sideband logic coupled to the phase compensation circuit via the control signal line and configurable to provide the control signal.

58. (Withdrawn) A memory device, comprising:

a memory core;

a memory transaction circuit coupled to the memory core and configurable to access the memory core; and

a data path coupled to the memory core and the memory transaction circuit, the data path configurable to perform a memory transaction between the memory core and one or more data lines in response to a control signal from the memory transaction circuit, wherein the data path is activated by the memory transaction circuit after a predetermined latency corresponding to when data is available on the one or more data lines.

59. (Withdrawn) The memory device of claim 58, wherein the memory transaction is a column access operation.

60. (Withdrawn) The memory device of claim 58, wherein the data path further comprises:

a receiver coupled to the memory transaction circuit and the one or more data lines, the receiver configurable to receive data from the one or more data lines in response to the control signal.

61. (Withdrawn) The memory device claim 58, wherein the memory transaction circuit comprises:

a first control logic configurable to receive and process row data for specifying a row address and bank address of the memory core for the memory transaction and to generate an activation signal; and

a second control logic coupled to the first control logic and configurable to receive and process data for specifying a column address and a column access operation, wherein the second control logic is activated by the activation signal generated by the first control logic in response to receipt of the row data.